Answer on Question #50353, Physics, Electric Circuits

Consider a D-type flip-flop.
The input to D changes from a logic 1 to a logic 0 just after the falling edge of the clock.
Qn=1 at the time D changes. Which of the following is true?

1. at the falling edge of the clock, Qn+1=0

2.at the falling edge of the clock, Qn+1=1

3.at the rising edge of the clock, Qn+1=0

4.at the rising edge of the clock, Qn+1=1

Answer:

D-type flip-flop has truth table, shown below:

(c) *D* Flip-Flop

D	$Q(t+1)$	Operation
0	0	Reset
1	1	Set

That's why at the falling edge of the clock, Q(n+1) will be equal to 0.