# Answer on Question #50352, Physics, Electric Circuits

**Task:**

Consider a J-K flip-flop. J=1, K=1. Which of the following is true?

1.at the falling edge of the clock, $Q_{n+1}$ is the same logic state as $Q_n$

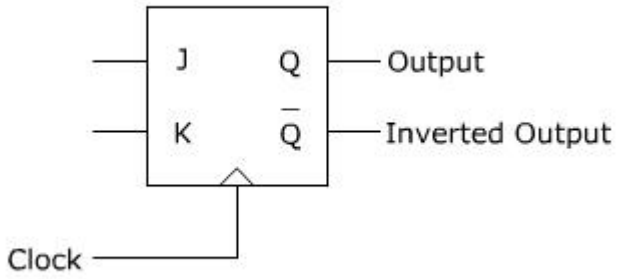
2.at the falling edge of the clock, $Q_{n+1}$ is the opposite state of $Q_n$

3.at the rising edge of the clock, $Q_{n+1}$ is the same logic state as $Q_n$

4.at the rising edge of the clock, $Q_{n+1}$ is the opposite state of $Q_n$

**Answer:**

The JK type flip-flop consists of two data inputs: J and K, and one clock input. There are again two outputs Q and Q' (where Q' is the reverse of Q).




The J-K flip-flop has its next output state decided by the state of its J and K inputs:

- If J= K= 0 the outputs do not change.
- If J = I and K = 0, the Q output becomes 1.
- If J = 0 and K = 1, the Q output becomes 0.
- If J = K = 1, the outputs change to the opposite state.

The $\overline{Q}$ output is always the inverse of the Q output. With most J-K flip-flops, the changes occur on the next rising edge of the clock. In the fourth case above, in which J = K = 1, we say that the outputs toggle on each rising edge.

**So the answer is 4.at the rising edge of the clock, $Q_{n+1}$ is the opposite state of $Q_n$**